

What is claimed is:

- 1 1. A method for enhancing the security of a system operating in conjunction with
2 a clock signal from a system clock, comprising:
3 monitoring the system for detecting a fault in the system;
4 upon detection of a fault, switching the system from operating in conjunction with
5 a clock signal from the system clock to operate in conjunction with a secure clock signal
6 from a secure clock.
- 1 2. The method of claim 1, wherein the system is switched to operate in conjunction
2 with a secure clock signal from one of a plurality of secure clocks.
- 1 3. The method of claim 1, further comprising:
2 monitoring the system operating in conjunction with a clock signal from a secure
3 clock,
4 upon detecting cessation of said fault in the system, switching the system to again
5 operate in conjunction with a clock signal from the system clock.
- 1 4. The method of claim 3, further comprising switching the system back to the clock
2 signal from the system clock even if the system clock is not operating.
- 1 5. The method of claim 1 further comprising monitoring the system for detecting a
2 fault associated with one of an over-frequency and under-frequency clock signals from
3 the system clock.
- 1 6. The method of claim 1, further comprising:
2 when switching the system to operate in conjunction with the secure clock signal
3 from the secure clock, preventing the clock signal from having short transitions that do
4 not cross the logic threshold from a high to low state or a low to high state.

1 7. The method of claim 1, wherein when switching from the clock signal of the
2 system clock to the secure clock signal of the secure clock, the clock signal has an extend
3 low time.

1 8. The method of claim 1 further comprising multiplexing together clock signals
2 from the system clock and from at least one secure clock and, upon detecting a fault,
3 selecting one of the multiplexed clock signals for operating the system.

1 9. The method of claim 3 further comprising, when switching between clock signals,
2 waiting until the clock signal, which is being switched from, transitions to a low state.

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1 10. An apparatus for enhancing the security of a system operating in conjunction with
2 a clock signal from a system clock, the apparatus comprising:
3 a secure clock generating a secure clock signal;
4 a clock monitor circuit configured to monitor the system for detecting a fault;
5 clock switching circuitry, the clock switching circuitry operably coupled to the
6 clock monitor circuit, the system clock signal and the secure clock signal;
7 the clock switching circuitry configured, upon the detection of a fault, to switch
8 the system from operating in conjunction with a clock signal from the system clock to
9 operate in conjunction with a secure clock signal from a secure clock.

1 11. The apparatus of claim 10, further comprising:
2 a plurality of secure clocks with secure clock signals;
3 the clock switching circuitry operably coupled to plurality of secure clock signals
4 for switching the system to operate in conjunction with one of the secure clock signals.

1 12. The apparatus of claim 10, wherein the secure clock includes a ring oscillator.

1 13. The apparatus of claim 10, wherein the clock monitor circuit is configured to
2 detect the cessation of the detected fault;
3 the clock switching circuitry further configured to switch the system to again
4 operate in conjunction with a clock signal from the system clock upon detecting the
5 cessation of said fault.

1 14. The apparatus of claim 10 wherein the clock monitor circuit is configured to
2 monitor the system for detecting a fault associated with one of an over-frequency and
3 under-frequency clock signals from the system clock, the clock switching circuitry
4 configured to switch the system to operate in conjunction with a secure clock signal from
5 a secure clock to prevent over-frequency and under-frequency clocking of the system.

1 15. The apparatus of claim 14 wherein the clock monitor circuit includes frequency
2 dividers; and, delay lines, the frequency dividers and delay lines configured to detect
3 over-frequency and under-frequency clock signals from the system clock.

- 1 16. An application specific integrated circuit comprising:
 - 2 a processor;
 - 3 a clock generating a system clock signal for operation of the processor;
 - 4 the secure clock further generating a secure clock signal;
 - 5 a clock monitor circuit configured to monitor the application specific integrated
 - 6 circuit
 - 7 for detecting a fault;
 - 8 clock switching circuitry, the clock switching circuitry operably coupled to the
 - 9 clock monitor circuit, the system clock signal and the secure clock signal;
 - 10 the clock switching circuitry configured, upon the detection of a fault, to switch
 - 11 the processor from operating in conjunction with a system clock signal to operating in
 - 12 conjunction with the secure clock signal.

1 17. The circuit of claim 16, further comprising:
2 a plurality of secure clocks with secure clock signals;
3 the clock switching circuitry operably coupled to plurality of secure clock signals
4 for switching the system to operate in conjunction with one of the secure clock signals.

1 18. The circuit of claim 16, wherein the clock monitor circuit is configured to detect
2 the cessation of the detected fault;
3 the clock switching circuitry further configured to switch the processor to again
4 operate in conjunction with the system clock signal upon detecting the cessation of said
5 fault.

1 19. The circuit of claim 16 wherein the clock monitor circuit is configured to monitor
2 the circuit for detecting a fault associated with one of an over-frequency and under-
3 frequency system clock signal, the clock switching circuitry configured to switch the
4 processor to operate in conjunction with a secure clock signal from a secure clock to
5 prevent over-frequency and under-frequency clocking of the processor.